AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for forming a self-aligned low temperature polysilicon thin film transistor (LTPS TFT), the method comprising the steps of:

providing a substrate comprising an N type LTPS TFT region and a P type LTPS TFT region;

sequentially forming a patterned undoped polysilicon layer, a dielectric layer, [[and]] a patterned conductive layer, and a first patterned photo resist layer, the patterned conductive layer and the first patterned photo resist layer comprising two first gaps in the N type LTPS TFT region;

performing a first implantation process to implant N type dopants via the first gaps into the undoped patterned polysilicon layer to form a source and a drain of an N type LTPS TFT;

performing a trimming process to remove a certain width of the first patterned photo resist layer;

removing ~~a certain width of~~ the patterned conductive layer not covered by the first patterned photo resist layer to form two second gaps and to define a gate of [[an]] the N type LTPS TFT;

performing a second implantation process to implant N type dopants via the second gaps into the undoped patterned polysilicon layer to form two lightly doped drains of the N type LTPS TFT;

forming a gate of a P type LTPS TFT in the P type LTPS TFT region; and

forming a source and a drain of the P type LTPS TFT in the P type LTPS TFT region.

2. (original) The method of claim 1 wherein the substrate is a glass substrate or a quartz substrate.

3. (original) The method of claim 1 wherein a buffer layer exists between the substrate and the patterned undoped polysilicon layer.

4. (currently amended) The method of claim 1 wherein the step of forming the patterned undoped polysilicon layer further comprises:

performing a sputtering process to form an amorphous silicon (α-Si) layer on the substrate;

performing an annealing process, such that the amorphous silicon layer is recrystallized and turned a polysilicon layer; and

performing a photo-etching process (PEP) to form [[a]] the patterned undoped polysilicon layer in each polysilicon layer of the N type LTPS TFT region and the P type LTPS TFT region.

5. (original) The method of claim 1 wherein the material of the dielectric layer comprises silicon oxide or silicon nitride.

6. (currently amended) The method of claim 1 wherein the step of forming the two first gaps and the two second gaps further comprises:

forming a [[first]] conductive layer and [[a]] the first patterned photo resist layer on the dielectric layer; and

removing the conductive layer that is not covered by the first patterned photo resist layer to form the two first

gaps in the conductive layer of the N type LTPS TFT region [[;]] .

~~performing a trimming process to reduce a certain width of the first patterned photo-resist;~~

~~removing the conductive layer that is not covered by the reduced first patterned photo-resist layer, such that the two second gaps are formed in the conductive layer of the N type LTPS TFT region; and~~

~~removing the reduced first patterned photo-resist layer.~~

7. (original) The method of claim 6 wherein the width of each first gap is smaller than the width of each second gap.

8. (original) The method of claim 6 wherein the material of the conductive layer is selected from the group consisting of aluminum, wolfram, chromium, and molybdenum.

9. (original) The method of claim 6 wherein the trimming process comprises an ash process, a descum process, and an ultraviolet beaming process or a thermal curing process.

10. (original) The method of claim 1 wherein the dopant concentration in the first implantation process is about 1E14 to 1E16 atoms/cm^2, and the N type dopants comprise arsenic or phosphorous.

11. (original) The method of claim 1 wherein the dopant concentration in the second implantation process is about 1E12 to 1E14 atoms/cm^2, and the N type dopants comprise arsenic or phosphorous.

12. (original) The method of claim 1 wherein the step of forming the gate of the P type LTPS TFT further comprises:

forming a second patterned photo resist layer to cover the gate of the N type LTPS TFT and parts of the P type LTPS TFT region for defining the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the second patterned photo resist layer, such that the gate of the P type LTPS TFT is formed; and

removing the second patterned photo resist layer.

13. (original) The method of claim 12 wherein the step of forming the source and the drain further comprises:

forming a third patterned photo resist layer, the third patterned photo resist layer covering the gate of the P type LTPS TFT;

performing a third implantation process to implant P type dopants to form the source and the drain of the P type LTPS TFT; and

removing the third patterned photo resist layer.

14. (original) The method of claim 13 wherein the dopant concentration in the third implantation is about 1E14 to 1E16 atoms/cm^2, and the P type dopants comprise boron or boron fluoride (BF_2).

15. (original) The method of claim 1 wherein the step of forming the gate, the source, and the drain of the P type LTPS TFT further comprises:

forming a fourth patterned photo resist layer, the fourth photo resist layer covering the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the fourth patterned photo resist layer, such that the gate of the P type LTPS TFT is formed.

performing a fourth implantation process to form the source and the drain of the P type LTPS TFT;

removing the fourth patterned photo resist layer;

forming a fifth patterned photo resist layer to cover the gate of the N type LTPS TFT and the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the fifth patterned photo resist layer; and

removing the fifth patterned photo resist layer.

16. (original) The method of claim 1 wherein the N type LTPS TFT is installed in a pixel array area of the substrate as a switching device of a pixel cell of an LCD.

17. (original) The method of claim 16 wherein the P type LTPS TFT and the N type LTPS TFT are low temperature polysilicon complementary metal-oxide-semiconductor thin film transistors (LTPS CMOS TFTs), and are installed in a periphery circuit area of the LCD as a logic device of the periphery circuit of the LCD.

18. (withdrawn) A method for forming a self-aligned low temperature polysilicon thin film transistor (LTPS TFT), the method comprising the steps of:

providing a substrate comprising an N type LTPS TFT region and a P type LTPS TFT region;

sequentially forming a patterned undoped polysilicon layer, a dielectric layer, a conductive layer, and a first patterned photo resist layer, the first patterned photo resist layer

comprising two first gaps;

performing an isotropic etching process to remove parts of the conductive layer via the two first gaps to form two second gaps, and to form a gate of an N type LTPS TFT;

implanting N type dopants into the patterned undoped polysilicon layer of the N type LTPS TFT region to form a source and a drain of the N type LTPS TFT;

removing the first patterned photo resist layer;

implanting N type dopants into the patterned undoped polysilicon layer of the N type LTPS TFT region to form two lightly doped drains (LDD) of the N type LTPS TFT;

forming a gate of a P type LTPS TFT in the P type LTPS TFT region; and

forming a source and a drain of the P type LTPS TFT in the P type LTPS TFT region.

19. (withdrawn) The method of claim 18 wherein the substrate is a glass substrate of a quartz substrate.

20. (withdrawn) The method of claim 18 wherein a buffer layer exists between the substrate and the patterned undoped polysilicon layer.

21. (withdrawn) The method of claim 18 wherein the step of forming the patterned undoped polysilicon layer further comprises:

performing a sputtering process to form an amorphous silicon (α-Si) layer on the substrate;

performing an annealing process, such that the amorphous silicon layer is recrystallized and turned a polysilicon layer; and

performing a photo-etching process (PEP) to form a

patterned undoped polysilicon layer in both the N type LTPS TFT region and the P type LTPS TFT region.

22. (withdrawn) The method of claim 18 wherein the material of the dielectric layer comprises silicon oxide or silicon nitride.

23. (withdrawn) The method of claim 18 wherein the width of each first gap of the first patterned photo resist layer is smaller than the width of each second gap.

24. (withdrawn) The method of claim 18 wherein the material of the conductive layer is selected from the group consisting of aluminum, wolfram, chromium, and molybdenum.

25. (withdrawn) The method of claim 18 wherein the N type dopants comprise arsenic or phosphorous.

26. (withdrawn) The method of claim 18 wherein the P type dopants comprise boron or boron fluoride (BF_2).

27. (withdrawn) The method of claim 18 wherein the step of forming the gate of the P type LTPS TFT further comprises:

forming a first patterned photo resist layer to cover the gate of the N type LTPS TFT and parts of the P type LTPS TFT region for defining the gate of the P type LTPS TFT;

removing the conductive layer that is not covered by the first patterned photo resist layer, such that the gate of the P type LTPS TFT is formed; and

removing the first patterned photo resist layer.

28. (withdrawn) The method of claim 18 wherein the step of forming the source and the drain further comprises:

forming a second patterned photo resist layer on the substrate;

implanting P dopants into the patterned undoped polysilicon layer of the P type LTPS TFT region by utilizing the second patterned photo resist layer and the gate of the P type LTPS TFT as a mask, such that the source and the drain of the P type LTPS TFT are formed; and

removing the second patterned photo resist layer.

29. (withdrawn) The method of claim 18 wherein the step of forming the gate, the source, and the drain of the P type LTPS TFT further comprises:

forming a third patterned photo resist layer, the third photo resist layer exposing parts of the patterned undoped polysilicon layer of the P type LTPS TFT region;

removing the patterned conductive layer that is not covered by the third patterned photo resist layer to form the gate of the P type LTPS TFT;

implanting P dopants into the patterned undoped polysilicon layer of the P type LTPS TFT region by utilizing the gate of the P type LTPS TFT and the third patterned photo resist layer as a mask, such that the P type source and the drain of the P type LTPS TFT are formed;

removing the third patterned photo resist layer;

forming a fourth patterned photo resist layer to cover the gate of the N type LTPS TFT and the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the fourth patterned photo resist layer; and

removing the fourth patterned photo resist layer.

30. (withdrawn) The method of claim 18 wherein the N type LTPS TFT is installed in a pixel array area as a switching device of a pixel cell of an LCD.

31. (withdrawn) The method of claim 30 wherein the P type LTPS TFT and the N type LTPS TFT are low temperature polysilicon complementary metal-oxide-semiconductor thin film transistors (LTPS CMOS TFTs), and are installed in a periphery circuit area of the LCD as a logic device of the periphery circuit of the LCD.

32. (withdrawn) The method of claim 18 wherein the isotropic etching process is a wet etching process.

33. (new) A method for forming a self-aligned low temperature polysilicon thin film transistor (LTPS TFT), the method comprising the steps of:

providing a substrate divided into an N type LTPS TFT region and a P type LTPS TFT region, the substrate comprising a patterned polysilicon layer and a dielectric layer thereon;

sequentially forming a patterned conductive layer and a first patterned photo resist layer on the dielectric layer, the patterned conductive layer and the first patterned photo resist layer comprising two first gaps via which the dielectric layer is partially exposed in the N type LTPS TFT region;

forming a source and a drain of an N type LTPS TFT in the undoped patterned polysilicon layer via the first gaps;

performing a trimming process to remove a certain width

of the first patterned photo resist layer;

removing the patterned conductive layer not covered by the first patterned photo resist layer to form two second gaps and to define a gate of the N type LTPS TFT;

forming two lightly doped drains of the N type LTPS TFT in the undoped patterned polysilicon layer via the second gaps; and

forming a gate, a source, and a drain of a P type LTPS TFT.

34. (new) The method of claim 33 wherein the substrate is a glass substrate or a quartz substrate.

35. (new) The method of claim 33 wherein a buffer layer exists between the substrate and the patterned undoped polysilicon layer.

36. (new) The method of claim 33 wherein the step of forming the patterned undoped polysilicon layer further comprises:

performing a sputtering process to form an amorphous silicon (α-Si) layer on the substrate;

performing an annealing process, such that the amorphous silicon layer is recrystallized and turned a polysilicon layer; and

performing a photo-etching process (PEP) to form the patterned undoped polysilicon layer in the N type LTPS TFT region and the P type LTPS TFT region.

37. (new) The method of claim 33 wherein the material of the dielectric layer comprises silicon oxide or silicon nitride.

38. (new) The method of claim 33 wherein the step of forming

the two first gaps further comprises:

forming a conductive layer and the first patterned photo resist layer on the dielectric layer; and

removing the conductive layer that is not covered by the first patterned photo resist layer to form the two first gaps in the conductive layer of the N type LTPS TFT region.

39. (new) The method of claim 38 wherein the width of each first gap is smaller than the width of each second gap.

40. (new) The method of claim 38 wherein the material of the conductive layer is selected from the group consisting of aluminum, wolfram, chromium, and molybdenum.

41. (new) The method of claim 33 wherein the trimming process comprises an ash process, a descum process, and an ultraviolet beaming process or a thermal curing process.

42. (new) The method of claim 33 wherein the source and the drain of the N type LTPS TFT are formed by performing a first implantation process in which dopants comprise arsenic or phosphorous with a concentration of 1E14 to 1E16 atoms/cm^2 are used.

43. (new) The method of claim 33 wherein the lightly doped drains of the N type LTPS TFT are formed by performing a second implantation process in which dopants comprise arsenic or phosphorous with a concentration of 1E12 to 1E14 atoms/cm^2 are used.

44. (new) The method of claim 33 wherein the step of forming the gate of the P type LTPS TFT further comprises:

forming a second patterned photo resist layer to cover the gate of the N type LTPS TFT and parts of the P type LTPS TFT region for defining the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the second patterned photo resist layer, such that the gate of the P type LTPS TFT is formed; and

removing the second patterned photo resist layer.

45. (new) The method of claim 44 wherein the step of forming the source and the drain of the P type LTPS TFT further comprises:

forming a third patterned photo resist layer covering the gate of the P type LTPS TFT;

performing a third implantation process to implant P type dopants to form the source and the drain of the P type LTPS TFT; and

removing the third patterned photo resist layer.

46. (new) The method of claim 45 wherein a dopant concentration in the third implantation is about 1E14 to 1E16 atoms/cm^2, and the P type dopants comprise boron or boron fluoride (BF_2).

47. (new) The method of claim 33 wherein the step of forming the gate, the source, and the drain of the P type LTPS TFT further comprises:

forming a fourth patterned photo resist layer;

removing the patterned conductive layer that is not covered by the fourth patterned photo resist layer, such that the gate of the P type LTPS TFT is formed;

performing a fourth implantation process to form the source and the drain of the P type LTPS TFT;

removing the fourth patterned photo resist layer;

forming a fifth patterned photo resist layer to cover the gate of the N type LTPS TFT and the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the fifth patterned photo resist layer; and

removing the fifth patterned photo resist layer.

48. (new) The method of claim 33 wherein the N type LTPS TFT is installed in a pixel array area of the substrate as a switching device of a pixel cell of an LCD.

49. (new) The method of claim 48 wherein the P type LTPS TFT and the N type LTPS TFT are low temperature polysilicon complementary metal-oxide-semiconductor thin film transistors (LTPS CMOS TFTs), and are installed in a periphery circuit area of the LCD as a logic device of the periphery circuit of the LCD.

50. (new) A method for forming a self-aligned low temperature polysilicon thin film transistor (LTPS TFT), the method comprising the steps of:

providing a substrate comprising a patterned polysilicon layer and a dielectric layer thereon;

sequentially forming a patterned conductive layer and a first patterned photo resist layer on the dielectric layer, the patterned conductive layer and the first patterned photo resist layer comprising two first gaps via which the dielectric layer is partially exposed in an N type LTPS TFT region;

forming a source and a drain of an N type LTPS TFT in the undoped patterned polysilicon layer via the first gaps;

performing a trimming process to remove a certain width of the first patterned photo resist layer;

removing the patterned conductive layer not covered by the first patterned photo resist layer to form two second gaps and to define a gate of the N type LTPS TFT; and

forming two lightly doped drains of the N type LTPS TFT in the undoped patterned polysilicon layer via the second gaps.

51. (new) The method of claim 50 wherein the substrate is a glass substrate or a quartz substrate.

52. (new) The method of claim 50 wherein a buffer layer exists between the substrate and the patterned undoped polysilicon layer.

53. (new) The method of claim 50 wherein the step of forming the patterned undoped polysilicon layer further comprises:

performing a sputtering process to form an amorphous silicon (α-Si) layer on the substrate;

performing an annealing process to turn the amorphous silicon layer into a polysilicon layer; and

performing a photo-etching process (PEP) to form the patterned undoped polysilicon layer.

54. (new) The method of claim 50 wherein the material of the dielectric layer comprises silicon oxide or silicon nitride.

55. (new) The method of claim 50 wherein the step of forming the two first gaps further comprises:

forming a conductive layer and the first patterned photo resist layer on the dielectric layer; and

removing the conductive layer not covered by the first patterned photo resist layer to form the two first gaps in the conductive layer of the N type LTPS TFT region.

56. (new) The method of claim 55 wherein the width of each first gap is smaller than the width of each second gap.

57. (new) The method of claim 55 wherein the material of the conductive layer is selected from the group consisting of aluminum, wolfram, chromium, and molybdenum.

58. (new) The method of claim 50 wherein the trimming process comprises an ash process, a descum process, and an ultraviolet beaming process or a thermal curing process.

59. (new) The method of claim 50 wherein the source and the drain of the N type LTPS TFT are formed by performing a first implantation process in which dopant comprise arsenic or phosphorous with a concentration of 1E14 to 1E16 atoms/cm^2 are used.

60. (new) The method of claim 50 wherein the lightly doped drains of the N type LTPS TFT are formed by performing a second implantation process in which dopants comprise arsenic or phosphorous with a concentration of 1E12 to 1E14 atoms/cm^2 are used.

61. The method of claim 50 wherein the substrate further comprises a P type LTPS TFT region.

62. The method of claim 61, further comprising forming a gate, a source, and a drain of a P type LTPS TFT in the P type LTPS

TFT region.

63. (new) The method of claim 62 wherein the step of forming the gate of the P type LTPS TFT further comprises:

forming a second patterned photo resist layer to cover the gate of the N type LTPS TFT and parts of the P type LTPS TFT region for defining the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the second patterned photo resist layer, such that the gate of the P type LTPS TFT is formed; and

removing the second patterned photo resist layer.

64. (new) The method of claim 63 wherein the step of forming the source and the drain of the P type LTPS TFT further comprises:

forming a third patterned photo resist layer covering the gate of the P type LTPS TFT;

performing a third implantation process to implant P type dopants to form the source and the drain of the P type LTPS TFT; and

removing the third patterned photo resist layer.

65. (new) The method of claim 64 wherein a dopant concentration in the third implantation is about 1E14 to 1E16 atoms/cm^2, and the P type dopants comprise boron or boron fluoride (BF_2).

66. (new) The method of claim 62 wherein the step of forming the gate, the source, and the drain of the P type LTPS TFT further comprises:

forming a fourth patterned photo resist layer;

removing the patterned conductive layer that is not

covered by the fourth patterned photo resist layer, such that the gate of the P type LTPS TFT is formed;

performing a fourth implantation process to form the source and the drain of the P type LTPS TFT;

removing the fourth patterned photo resist layer;

forming a fifth patterned photo resist layer to cover the gate of the N type LTPS TFT and the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the fifth patterned photo resist layer; and

removing the fifth patterned photo resist layer.

67. (new) The method of claim 50 wherein the N type LTPS TFT is installed in a pixel array area of the substrate as a switching device of a pixel cell of an LCD.

68. (new) The method of claim 62 wherein the P type LTPS TFT and the N type LTPS TFT are low temperature polysilicon complementary metal-oxide-semiconductor thin film transistors (LTPS CMOS TFTs), and are installed in a periphery circuit area of the LCD as a logic device of the periphery circuit of the LCD.